Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N.1R**
2. **1D**
3. **1CP**
4. **N.1S**
5. **1Q**
6. **N.1Q**
7. **GND**
8. **N.2Q**
9. **2Q**
10. **N.2S**
11. **2CP**
12. **2D**
13. **N.2R**
14. **VCC**

**.051”**

**.055”**

**11**

**10**

**2 1 14 13 12**

**3**

**4**

**5 6 7 8 9**

**HCT**

**74T**

**MASK**

**REF**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .004” X .004”**

**Backside Potential: Vcc**

**Mask Ref: HCT74T**

**APPROVED BY: DK DIE SIZE .051” X .055” DATE: 4/25/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HCT74**

**DG 10.1.2**

#### Rev B, 7/19/02